Advanced Verification Solutions for ICs to Ensure High Quality Amid PVT Variations

Presentation by
Lih-Jen Hou, Product Manager, **Siemens**

SIEMENS THine

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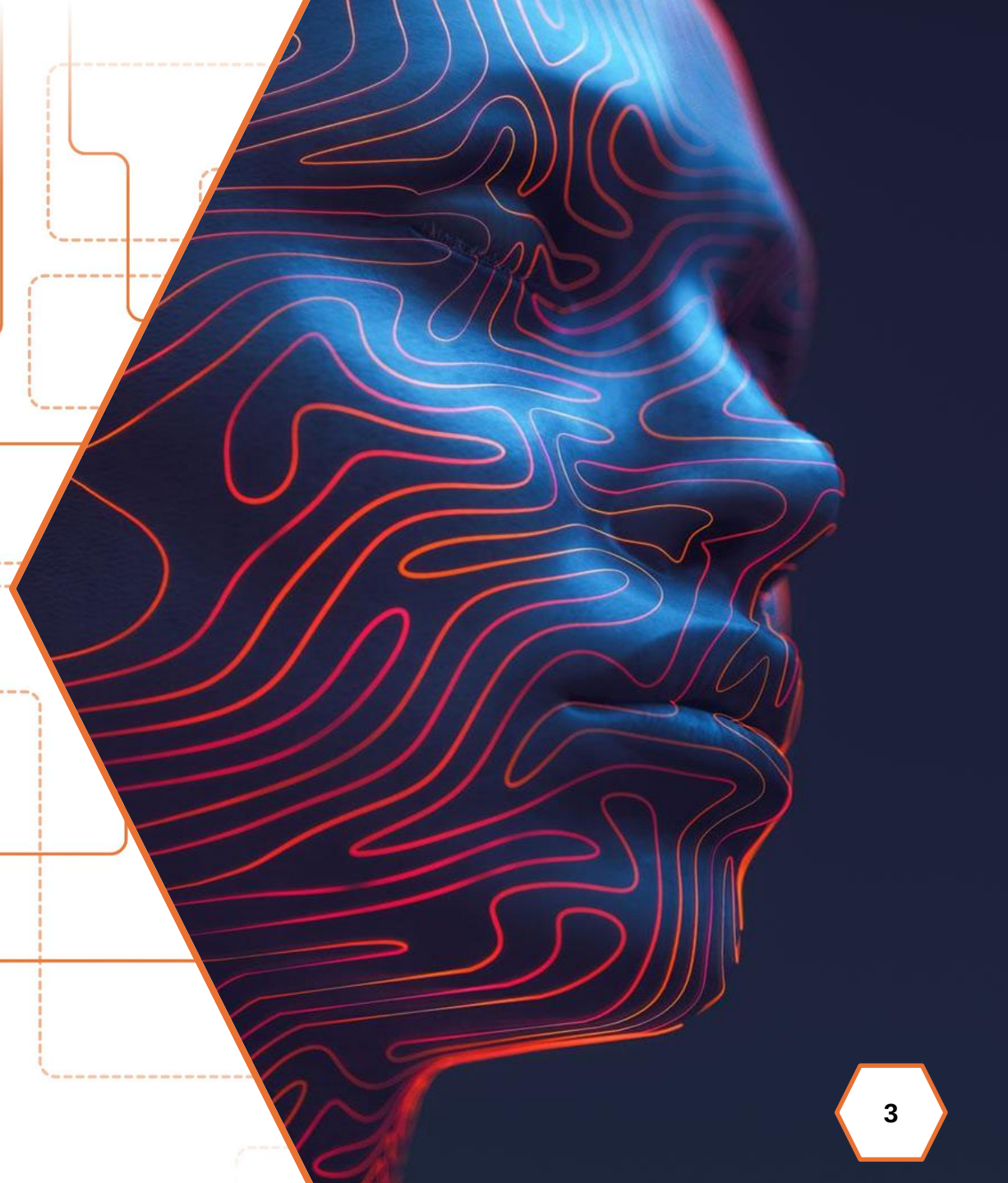
Lih-Jen Hou

Product Manager,
Siemens EDA

In This Presentation

We will explore the complex verification challenges encountered in a communication system

*Also, we will elaborate on the methodology used to overcome them, and the achieved results, highlighting how the collaboration between **THine Electronics** and **Siemens EDA** leveraged an AI-powered design verification flow including **Solido Simulation Suite** and **Solido Design Environment** to achieve accurate results with remarkable efficiency gains.*



Motivation

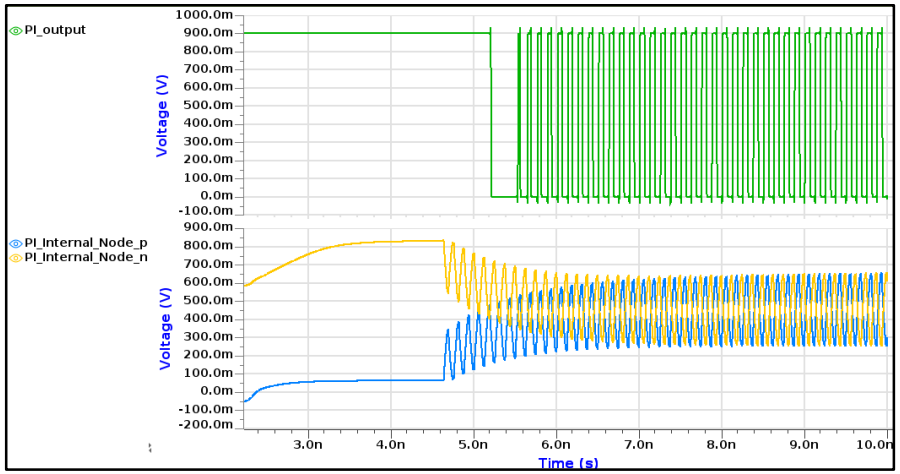
Addressing verification challenges on Phase Interpolators (PIs) in a communication system

- Sampling clock timing is controlled by phase interpolator(PI) with high resolution
- The accuracy of the PI is crucial to the stability of the communication system
- In this presentation, ADC requires 8 outputs for 8-interleaving sampling, and the phase shift between clocks greatly affects the stability of the communication, so a PI with no variation is desired.

Motivation

Addressing verification challenges on Phase Interpolators (PIs) in a communication system

- Both single simulation time and overall design cycle are extremely long
  - Multiple PIs have large circuit sizes
  - PIs take a long time in transient simulation to stabilize output
  - Statistical simulation is needed to verify the impact of manufacturing variations

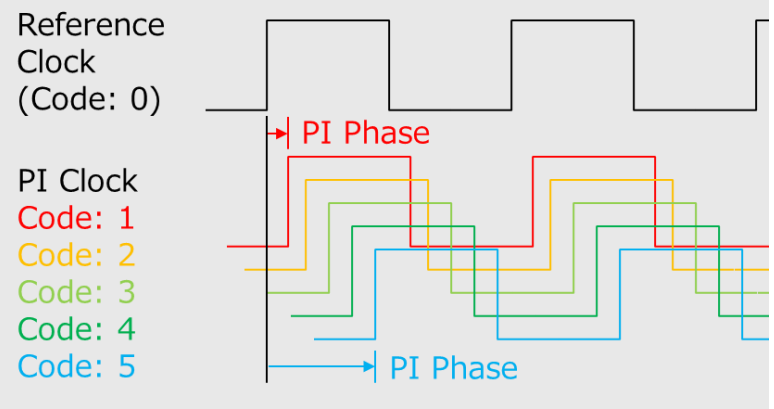


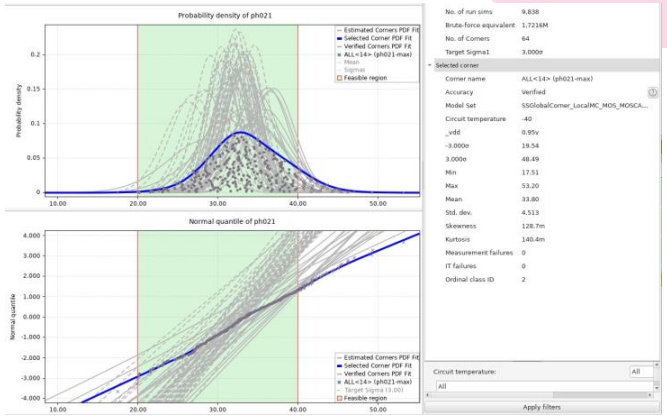
Waveform example for PI simulation

A revolutionary simulation flow significantly enhances communication system verification

Main Idea

Achieving Efficient Verification Flow by Integrating Diverse Simulation Tools





- An accurate SPICE simulator is essential for ensuring the precision of single-point simulations
- An AI-powered simulation flow enables variation-aware simulations with a reasonable number of runs

Schematic	Pre-Sim	Layout / Extraction	Post-Sim	Variation-Aware Sim
Design Platform	**Solido Sim Solido DE**	Calibre Platform	**Solido Sim Solido DE**	**Solido Sim PVTMC Verifier**

Solido Simulation Suite: Ensures design accuracy with each simulation
Solido Design Environment: Intuitive GUI for easier building of simulation states

Solido Simulation Suite: Optimized solver and RC reduction algorithm keeps post-sim efficient
PVTMC Verifier: Statistical simulations with multiple corners in one-shot, with brute-force level accuracy

Main Idea

Solido Simulation Suite with Solido Design Environment ensures the design quality

Design environment, SPICE simulation and embedded post-processing for circuit design and verification

Solido Design Environment

- SPICE-accurate, AI-powered nominal & variation analysis
- Sweeps and measurements
- Waveform analysis with post-processing

AFS, Solido Simulation Suite

- AI-accelerated simulators for intelligent design and verification
- High accuracy, high performance, pre- and post- layouts
- Full-spectrum & multi-tone analyses

Foundry-certified PDKs

TSMC, Samsung, GlobalFoundries, Intel, UMC, Tower, STMicroelectronics

SPICE syntax-agnostic

Spectre, HSPICE, Eldo

Supports industry-standard outputs

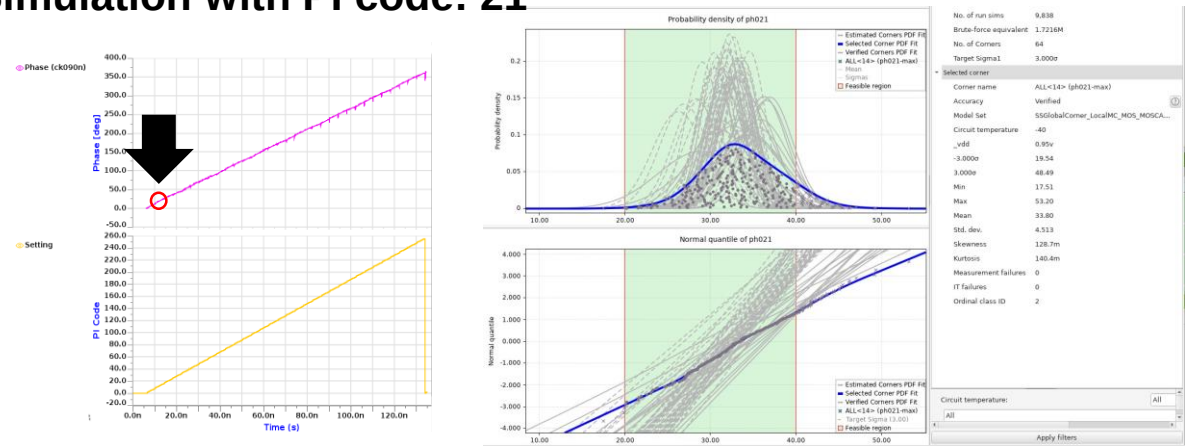
Full-featured analysis for RF

DC/AC/Transient/Monte-Carlo/PSS/HB/S-parameter/Sweep/Noise/Aging

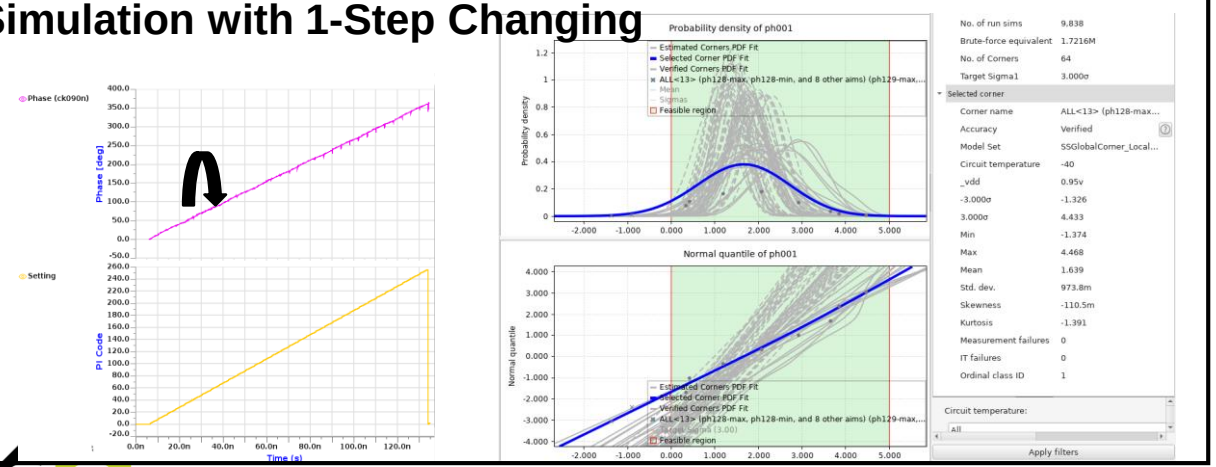
Evidence

Stability and yield needs to verify, for alleviating manufacturing variation

Simulation with PI code: 21



Simulation with 1-Step Changing



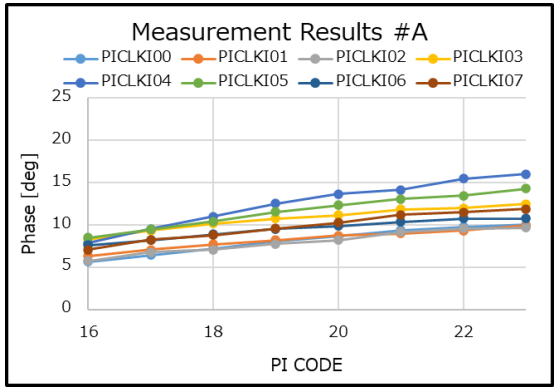
- Detailed verification with various PVT corners as well as statistical samples to verify the phase shift value for each code, or between two codes, is crucial
- Manufacturing variation might cause the instability to impact the overall accuracy and performance
- Siemens' PVTMC Verifier provides the solution for overall verification among all designated corners, including PVT conditions

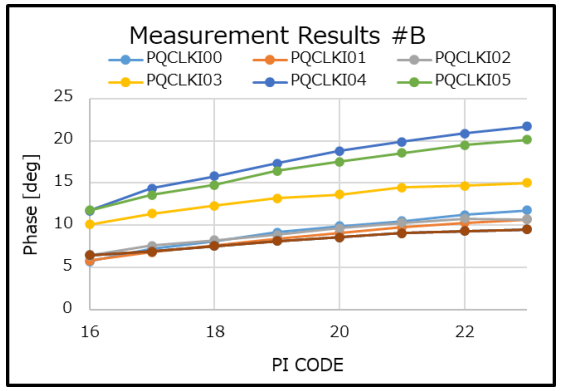
Code Setting	Target Sigma	Brute Force (CI ~0.1σ)	PVTMC (CI ~0.1σ)
PI Code: 21	3σ	1.72M sims (multiple corner)	**9838 sims (multiple-Corners)**
1-Step Changing	3σ		

Evidence

Statistical results perfectly aligns with the variation-aware simulation

Silicon Measurement Results





Code Setting	1σ Sim Result	1σ Meas Result
PI Code: 21	3.1 degree	3.4 degree
1-Step Changing	0.62 degree	0.42 degree

- Various chips with different measurement result with PVT corners are necessary to emulate the real scenario
- From the result in the table, measurement with statistical result aligned with the simulation results

Summary

THine has designed a new phase interpolator to improve their communication system

- The accuracy of the phase interpolator is crucial to the entire design
- Manufacturing variation may cause a huge impact on the final output

Siemens EDA has collaborated with THine on an AI-powered design flow to achieve accurate, efficient simulation in the design cycle

- AFS, part of Solido Simulation Suite, for analog verification provides significant performance gains without compromising accuracy
- PVTMC Verifier, part of Solido Design Environment, for variation-aware simulations provides the most efficient way to cover all possible scenarios of corners, ensuring the quality of manufactured chips

AI-powered simulation flows greatly enhance performance while maintaining accuracy

This work was supported in part by the **Ministry of Internal Affairs and Communications of Japan** (*JPJ000254, Research and Development for Expansion of Radio Wave Resources*)